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NOISE GAIN CONTROL

BACKGROUND

5   **I. Field of the Invention**

The present invention relates to communications. More particularly, the present invention relates to a novel and improved method and apparatus for automatic gain control in a communications receiver.

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II. Description of the Related Art

Wireless devices utilize radio waves to provide long distance communications without the physical constraints of a wire-based system.
15   Information is provided to devices using radio waves transmitted over predetermined frequency bands. Allocation of available frequency spectrum is regulated to enable numerous users access to communications without undue interference.

A remote receiver tuned to a carrier frequency is required to receive and
20   demodulate signals transmitted from a corresponding transmitter at the same carrier frequency. The remote receiver recovers the baseband signal from the modulated carrier. The baseband signal may be directly presented to a user or may be further processed prior to being presented to the user.

A mobile receiver in a portable communication system operates in an
25   environment that subjects the receive signal to numerous degradations. The signal transmitted from a signal source is subject to numerous conditions, such as attenuation, interference, scattering, and reflections, prior to arrival at a receiver. The receiver must be able to recover the signal in spite of all these degradations in order for a successful communication link to be established.

30   Structures, such as buildings, and surrounding terrain, including walls and hillsides, contribute to the scattering and reflection of the transmitted signal. The scattering and reflection of the transmit signal results in multiple signal paths from the transmitter to the receiver. The contributors to the multiple signal paths change as the receiver moves.

35   Other signal sources also result in degradation of the desired signal. The other signal sources may be other transmitters intentionally operating on the same frequency as the desired signal as well as transmitters that generate spurious signals in the frequency band of the desired signal.

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Other sources of signal degradation are generated within the receiver itself. Signal amplifiers and signal processing stages within the receiver may degrade the level of the desired signal with respect to the level of thermal noise. The signal amplifiers and processors within the receiver may also generate
5   noise products or distort the received signal and further degrade its quality.

Receivers designed to operate within defined communication systems must be designed to operate in spite of all sources of signal degradation. In an exemplary embodiment, the wireless communication system may be a system such as a Code Division Multiple Access (CDMA) wireless system, consistent
10   with "Telecommunications Industry Association (TIA)/ Electronics Industries Association (EIA)/IS-2000 STANDARDS FOR CDMA2000 SPREAD SPECTRUM SYSTEMS" referred to as "the cdma2000 standard." In alternate embodiments, the system may be a system consistent with the "TIA/EIA/IS-95 MOBILE STATION-BASE STATION COMPATIBILITY STANDARD FOR
15   DUAL-MODE WIDEBAND SPREAD SPECTRUM CELLULAR SYSTEM," hereinafter referred to as "the IS-95 standard," or other systems such as described by American National Standards Institute (ANSI) "J-STD-008, PERSONAL STATION-BASE STATION COMPATIBILITY REQUIREMENTS FOR 1.8 TO 2.0 GHZ CODE DIVISION MULTIPLE ACCESS (CDMA)
20   PERSONAL COMMUNICATIONS SYSTEMS," or "ANSI J-STD-015 DRAFT STANDARD FOR W-CDMA (WIDEBAND CODE DIVISION MULTIPLE ACCESS) AIR INTERFACE COMPATIBILITY STANDARD FOR 1.85 TO 1.99 GHz PCS APPLICATIONS" referred to as "W-CDMA," or other systems generally referred to as High Data Rate (HDR) systems.

25   In addition to operating in a noisy environment, a receiver must be capable of handling input signals varying over a large range. A typical receiver operating in a system defined by one of the standards listed above must be capable of handling an input signal range of 100 dB or more. However, a typical signal amplifier remains linear over a much smaller range. A receiver
30   typically incorporates some form of gain control in order to maintain signal linearity at the later stages of the receiver. Gain control may take the form of switched amplifiers, variable gain amplifiers, or a combination of switched and variable gain amplifiers. Additionally, since a receiver may utilize both analog and digital stages, gain control may control the gain of analog stages of the
35   receiver prior to an Analog to Digital Converter (ADC) and may also control the gain of the signal in digital stages following the ADC.

The typical gain control circuit performs Automatic Gain Control (AGC), although it is possible to implement manual gain control in receivers having slowly varying signal levels. The AGC may be implemented using discrete

gain steps, constant variable gain, or a combination of the two. An AGC circuit, in a receiver having analog and digital stages, is typically implemented in the analog portion of the receiver in order to optimize the signal level input to the ADC. The AGC is configured such that the mean energy level of the received signal at the input to the ADC is maintained at a predetermined level. This predetermined signal level, termed the AGC set point, is typically chosen to be a number that results in ADC input signal levels near the middle of the ADC range. The design of the digital stages can be optimized to the AGC set point value. The bitwidths of subsequent digital stages may be optimized to the AGC set point. A higher AGC set point may require a larger bitwidth in the subsequent digital stages to ensure the signal does not saturate the digital processing stage. A lower AGC set point, correspondingly, may require a smaller bitwidth in subsequent digital stages. The actual bitwidths implemented in the digital portion of the receiver design are of greater interest when stages of the digital portion of the receiver are implemented within a single Integrated Circuit (IC). A larger bitwidth typically will require a larger physical area and the consumption of more resources within a single IC. Thus, it may be preferable to limit the bitwidths within an IC design to no greater than a minimum level.

The bitwidths of the subsequent digital stages will typically be designed to accommodate the worst case AGC set point when the AGC set point is allowed to vary over the whole range of the ADC. This results in an excessive bitwidth and the consumption of a limited amount of resources within the IC when a lower AGC set point is used in the receiver design.

A similar situation exists for receivers that implement analog stages following the AGC stages. In such a receiver the AGC set point is determined prior to subsequent analog stages. The subsequent analog stages may have limited dynamic ranges, as in the case of an amplifier. It is preferable to design the subsequent analog stages such that an amplifier is linear over the dynamic range determined by the AGC set point. It may not be desirable to implement an amplifier having a dynamic range far exceeding that determined by the AGC set point since both physical space and excessive power is consumed. However, when the AGC set point is allowed to vary over a predetermined range, the subsequent analog stages will typically be designed to accommodate the worst case AGC set point.

In both the digital and analog designs the subsequent stages are typically designed to accommodate the worst case4 AGC set point. If the actual AGC set point of the receiver is not designed to be the worst case AGC set point the result is a non-optimal design for the subsequent stages and the use of

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excessive resources. What is needed is a method and apparatus for making the receiver design insensitive to the AGC set point value.

SUMMARY

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      The present embodiments disclose a novel noise gain control method and apparatus in a communications receiver that allows receiver operation to be insensitive to a predetermined AGC set point. A noise gain controller is provided at a copy of the received signal following the AGC stages. A noise

10 estimator is used to determine an estimate of the noise in the received signal. The noise estimate is coupled to a noise gain discriminator that processes the noise estimate. The noise gain discriminator transforms the noise estimate into an error signal. The output of the noise gain discriminator is coupled to a filter that is used to establish the time constant of the noise controller loop. In one

15 embodiment, the filter is a lowpass filter. The output of the filter is coupled to an accumulator. The accumulator is used to accumulate error signals into a composite error signal. The composite error signal is applied to a multiplier that scales the received signal following the AGC stages.

      In a first embodiment, the received signal following the AGC is a CDMA

20 signal having quadrature components. The noise estimator is comprised of a despreading and Walsh code decovering stage. This stage of the noise estimator despreads the signal using a Walsh code not assigned to any of the channels within the communication system. In one embodiment, the Walsh code is sixteen chips long. The despread output is coupled to an accumulator.

25 In an embodiment, the accumulator accumulates the signal over a period equal to the length of the Walsh code. In a particular embodiment, the accumulator accumulates the noise over sixteen chips. The output of the accumulator is coupled to a noise energy calculator that calculates the noise energy output from the accumulator. The output of the noise energy calculator is coupled to

30 an energy accumulator. The energy accumulator sums the output from the noise energy calculator over a predetermined time. In an embodiment, the energy accumulator is a discrete accumulator that accumulates the calculated noise energy over a predetermined number of samples. The output of the noise energy accumulator represents the output of the noise estimator.

35 In another embodiment, the noise estimator is provided a CDMA signal having quadrature components. The first stage is a despreading and Walsh decovering stage as in the first embodiment. However, the despreader uses an arbitrary code. In one embodiment the code is ++--. The output of the

despreader is coupled to an accumulator that is adapted to accumulate the signal over the length of the despreading code.

BRIEF DESCRIPTION OF THE DRAWINGS

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The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

10 FIG. 1 is a block diagram of a wireless communication receiver;

FIG. 2 is a block diagram of a noise gain controller;

FIG. 3 is a block diagram of a noise estimator;

FIG. 4 is a block diagram of a noise estimator;

FIG. 5 is a flow chart of a noise gain control method; and

15 FIG. 6 is a flow chart of a noise estimator method.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 FIG. 1 shows a block diagram of a wireless receiver **100** such as may be used in a wireless phone. Although a receiver is shown in FIG. 1, it can be seen that the component parts may be combined with a transmitter to produce an integrated transceiver. Similarly, although a wireless receiver is shown in FIG. 1, a wire line device may be configured by eliminating the antenna or coupling 25 the antenna to a wire line connection.

An antenna **10** may be used to interface the receiver **100** to incoming radio waves. The antenna **10** may also be used to broadcast a signal if the receiver **100** is combined with a transmitter in a transceiver configuration. The output of the antenna **10** is coupled to a LNA **22**. The LNA **22** following the 30 antenna **20** is used to amplify the receive signal and may also represent the major contributor to the receiver's noise figure. The noise figure of the LNA **22** adds directly to the noise figure of the receiver while the noise figure of subsequent stages is reduced in proportion to the LNA **22** gain. Thus, the LNA **22** is typically chosen to provide a minimal noise figure in the receive band 35 while amplifying the receive signal with sufficient gain to minimize noise figure contributions from subsequent stages. There are competing design requirements, such as DC power requirements and device third order intercept point, that make the choice of LNA **22** gain a trade off of many design constraints. The signal amplified in the LNA **22** is coupled to an RF filter **24**.

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The RF filter **24** is used to provide rejection to signals outside of the receive band. The RF filter **24** is used after, rather than before, the first LNA **22** stage in order to reduce the filter's contribution to the receiver noise figure. The output of the RF filter **24** is coupled to a second LNA **26**. The second LNA **26** is used to

5   further amplify the received RF signal. A second LNA **26** stage is typically used where sufficient gain cannot be achieved in a single LNA stage while also satisfying third order intercept constraints although a single LNA may be sufficient in some receiver applications. The output signal from the second LNA **26** is coupled to an input of a RF mixer **30**.

10   The RF mixer **30** mixes the amplified receive signal with a signal generated within a first Local Oscillator (LO) **60** to downconvert the signal to an Intermediate Frequency (IF). The output of the first LO **60** is typically coupled to a buffer amplifier **62** prior to being coupled to the RF mixer **30**. The IF output of the RF mixer **30** is coupled to an IF amplifier **32** that is typically

15 used to increase the signal level. In the receiver embodiment shown in FIG. 1, the output of the RF mixer **30** and all subsequent signal processing stages utilize a balanced signal configuration. A balanced signal configuration may be preferred over a single ended configuration due to noise considerations.

       The IF amplifier **32** following the RF mixer **30** typically has limited

20 frequency response and does not amplify the upconverted signal that is output from the RF mixer **30**. The output of the IF amplifier **32** is coupled to an IF filter **34**. The IF filter **34** is used to filter the IF from a single receive channel. The IF filter **34** typically has a much narrower frequency response than does the RF filter **24**. The IF filter **32** can have a much narrower bandwidth since the RF

25 mixer **30** typically downconverts the desired RF channel to the same IF regardless of the frequency of the RF channel. In contrast, the RF filter **24** must pass the entire receive band since any channel in the receive band can be allocated to the communication link. The output of the IF filter **34** is coupled to a receive Automatic Gain Control (AGC) amplifier **36**.

30   The AGC amplifier **36** is used to maintain a constant amplitude receive signal for subsequent stages. The gain of the AGC amplifier **36** is varied using a control loop that detects the amplitude of the received signal. The output from the AGC amplifier **36** is coupled to a second downconversion stage as well as to the input to an Automatic Gain Controller (AGC) **70**. The AGC **70** in the

35 embodiment shown in FIG. 1 is coupled to the output of the AGC amplifier **36**. However, the input to the AGC **70** may be coupled to the output of a subsequent downconversion stage or a baseband stage. The AGC **70** outputs control signals to the amplifiers in the receive signal path in order to maintain a constant signal level at the input to the AGC **70**. Here, the AGC **70** outputs

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control signals to the LNAs, **22** and **26**, as well as to the AGC amplifier **36**. The AGC **70** controls the gain in the receive signal path such that the signal level at the input to the AGC **70** is relatively constant. The level that the AGC **70** attempts to maintain at its input is known as the AGC set point. The AGC **70** in
5   conjunction with the controlled amplifiers operate as a control loop to maintain the received signal near the AGC set point.

The output of the AGC amplifier **36** is also coupled to a second downconversion stage. In FIG. 1, the receiver **100** is configured to receive a quadrature modulated signal and the second downconversion stage utilizes
10   two mixers. A first IF mixer **42** downconverts the IF signal to a baseband signal. The second Local Oscillator (LO) **40** used in conjunction with the IF mixer **42** may be separate and distinct from the first LO **60**. The output of the second LO **40** is coupled to the first IF mixer **42**. The output of the first IF mixer **42** is designated as an in phase or I signal component of the received signal.
15   The I signal component of the received signal is coupled to a first Analog to Digital Converter (ADC) **52**. The digitized I signal component is coupled to the baseband processor **102**.

The output of the AGC amplifier **36** is also coupled to a second IF mixer **44**. A phase shifted version of the second LO **40** is used to drive the second IF
20   mixer **44**. The phase shifted LO is generated by coupling the output of the second LO **40** to a phase shifter **46** and then coupling the phase shifted output to the second IF mixer **44**. The LO signals driving the first IF mixer **42** and second IF mixer **44** are in quadrature when the phase shifter **46** provides ninety degrees of phase shift. The resultant output of the second IF mixer **44** is termed
25   the quadrature, or Q signal component, of the received signal since it is in quadrature with the I signal component. The Q signal component is then coupled to a second ADC **54** which digitizes the signal and couples the digitized signal to the baseband processor **102**.

The baseband processor **102** block represents subsequent signal
30   processing that is performed on the baseband signal. The subsequent baseband processing includes the noise gain control as described in detail below. Other examples of subsequent processing include, but are not limited to, despreading, deinterleaving, error correction, filtering, and amplification. The received information processed in the baseband processor **102** is then routed to the
35   appropriate destination. The information may be used within the receiver **100** or may be routed to a user interface such as a display, loudspeaker, or data port.

It may be seen that the signal amplitude at the ADC inputs, and thus at the baseband processor inputs, may be dependent upon the AGC set point.

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The AGC set point may be defined with respect to the composite signal power or may be defined with respect to the I and Q signal components when the signal is a quadrature modulated signal. In an embodiment where the received signal is a quadrature modulated signal, the AGC set point may be defined as
5   the sum of the squares of the I and Q components, or $I^2 + Q^2$. The receiver designer may arbitrarily assign the actual AGC set point value, although typically the determination is made using the dynamic range of the ADC. Different receiver designs using the same ADCs may incorporate different AGC set points, depending on design trade off investigated.

10   The digital signal processing stages following the AGC stage may be designed to be insensitive to the AGC set point by incorporating a Noise Gain Controller (NGC) 200 as shown in FIG. 2. The Noise Gain Controller (NGC) 200 is coupled to the receiver front end and operates as a signal processor on signals following the AGC stages. In FIG. 2, the NGC 200 is coupled to
15   Antenna Input RAM 202. The Antenna Input RAM 202 may represent a buffer that receives the ADC outputs from the initial signal processing stages of the receiver. Alternatively, the NGC 200 may be coupled to the ADCs and may receive the digitized receive signals with no buffering. In an analog configuration, the NGC 200 may be coupled to the final output stage of the
20   AGC loop. Regardless of the receiver configuration, the NGC 200 is typically configured to follow the AGC loop.

The initial signal processing element in the NGC 200 is a multiplier 210. The output of the Antenna Input RAM 202 is coupled to a first input of the multiplier 210. Alternatively, the initial signal processing element in the NGC
25   200 may be a signal summer having in phase signal inputs or a combination of in phase and inverted signal inputs. In another embodiment, the initial signal processing element in the NGC 200 may be a signal combining means having first and second inputs and an output that is a signal processed version of the inputs. The signal combining means may incorporate a predetermined transfer
30   function using the signals provided at the first and second inputs to generate an output. The output of the multiplier 210, or signal combining means, represents the corrected output of the NGC 200, and is coupled to the signal processing 250 stages that would normally follow the Antenna Input RAM 202 in the absence of a NGC 200. The output of the multiplier 210 is also coupled
35   within the NGC 200 to a Noise Estimator 220. The Noise Estimator 220 is used to extract an estimate of the noise level within the composite received signal. Particular embodiments of Noise Estimators 200 are provided in Figs 3 and 4 and are discussed in further detail below.

The output of the Noise Estimator **220** is coupled to a Noise Gain Discriminator **230**. The Noise Gain Discriminator **230** incorporates a predetermined transfer function to generate an output signal that represents an error signal, also known as a gain correction factor. In one embodiment, the

5 Noise Gain Discriminator **230** normalizes the noise estimate to a predetermined noise gain set point value and then calculates the inverse. In another embodiment, the Noise Gain Discriminator **230** calculates the difference between a predetermined noise gain set point value and the noise estimate. The predetermined noise gain set point value used in the Noise Gain

10 Discriminator **230** calculation is distinct from the AGC set point value used in the AGC loop. The noise gain set point may or may not have the same value as the AGC set point. The operation of the NGC **200** is not affected by the relative differences between the noise gain set point and AGC set point.

The output of the Noise Gain Discriminator **230** is coupled to a lowpass

15 filter **240**. The lowpass filter **240** is used to establish the loop bandwidth used in the NGC **200**. The lowpass filter **240** may be eliminated if the output of the Noise Gain Discriminator **230** is of the proper bandwidth or if signal filtering is incorporated into the transfer function of the Noise Gain Discriminator **230**. The output of the lowpass filter **240** is coupled to an error signal accumulator

20 **260**.

The error signal accumulator **260** comprises an error summer **262** having a first input coupled to the input to the error signal accumulator **260** and a second input coupled to the output of the error signal accumulator **260**. The output of the error summer **262** is coupled to a delay element **264**. The delay

25 element **264** may be implemented as a register, buffer, FIFO or any other means capable of delaying a signal. The output of the delay element **264** is also the output of the error signal accumulator **260** and is coupled to a second input of the multiplier **210**.

Thus, the scaled output of the multiplier **210** represents the input signal

30 to the NGC **200** corrected for the noise level. Where the noise gain discriminator **230** calculates the inverse ratio of the noise estimate to a predetermined noise gain set point value, the output of the NGC **200** is a signal normalized to the noise gain set point value. Thus, the noise gain set point value may represent the effective AGC set point value seen by all stages

35 subsequent to the NGC **200**.

In one embodiment the receiver is a CDMA receiver and the signal processing stages represent the baseband signal processing stages within a CDMA receiver. Each finger of a multi-finger rake receiver implemented within the CDMA receiver utilizes an independent NGC **200**. By normalizing

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the received signals to a predetermined noise gain set point, the signal processing stages may be optimized for the noise gain set point.

The AGC set point is based on the energy of all received channels and noise while the NGC set point is based only on noise. This is helpful when the
5   NGC and subsequent signal processing stages are implemented within a single Integrated Circuit (IC) and the IC is implemented within multiple receiver designs, each having their AGC set point independently determined during the design process.

FIG. 3 shows a block diagram of an embodiment of a Noise Estimator
10 **222** that may be used within a CDMA receiver. In a CDMA system, multiple channels are made orthogonal using Walsh codes. In general, each channel information symbols of a predetermined length. Each channel is assigned one of a plurality of orthogonal Walsh codes. A noise estimator may be designed by multiplying the received signal by a Walsh code that has not been assigned
15 to any information carrying signal.

The embodiment shown in FIG. 3 may be implemented within a CDMA receiver designed to receive signals in accordance with the cdma2000 standard, where the receiver is designed to receive the reverse link signals broadcast from a mobile station to a base station. However, it may be seen that the particular
20 implementation of the Noise Estimator **222** is not limited to this particular application.

The input signal to the Noise Estimator **222** is coupled to a Walsh Code Decover stage **310**. The reverse link in a communication system operating in accordance with the cdma2000 standard allows each mobile unit to generate
25 multiple simultaneous code channels through the use of Walsh codes. Multiple simultaneous code channels are allowed in some configurations of the cdma2000 standard reverse link using orthogonal Walsh codes. The received symbol may be recovered by despreading the received signal with the appropriate Walsh code. Symbols that do not correlate with the appropriate
30 Walsh code appear as noise. The Noise Estimator **222** uses the orthogonal properties of Walsh codes to generate a noise estimate of the received signal. The Walsh Code Decover stage **310** despreads and decovers the input signal using a Walsh code that is not assigned to any channel. In one embodiment, the Walsh code used to despread and decover the received signal is "++++-------
35 -++++", where binary signals are represented with "+" or "-" values and "+" may represent a "0" and "-" may represent a "1". The resultant output is an estimate of the noise in the received signal since the Walsh code used does not correspond to the Walsh code for any channel.

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The output of the Walsh Code Decover stage **310** is then coupled to a noise accumulator **320**. In the embodiment shown in FIG. 3 the noise accumulator **320** accumulates the output of the Walsh Code Decover stage **310** over the length of the Walsh code. The noise accumulator **320** in this

5   embodiment accumulates the noise estimate over sixteen samples, or chips, since the Walsh code length used to despread the signal is sixteen. Accumulating over the same number of chips as is used to spread the symbols results in an accumulation time of one symbol. The output of the noise accumulator **320** is coupled to an Energy Computation **330** where the

10   accumulated noise estimate is transformed into an energy value. In a CDMA receiver application, the input signal to the Noise Estimator **222** may be a quadrature signal. The Walsh Code Decover **310** and noise accumulator **320** may be configured to process both the I and Q components of the quadrature signal. In an embodiment there may be parallel processing stages for the I and

15   Q components, while in another embodiment the processing of the I and Q components may be time multiplexed.

Energy Computation **330** may calculate the energy of the accumulated quadrature signal by summing the squares of the I and Q components. The energy Computation **330** outputs I^2+Q^2 as the resultant energy value. The

20   output of the Energy Computation **330** is coupled to an Energy Accumulator **340** that is used to accumulate a predetermined number of calculated energy values. The Energy Accumulator **340** may be used to average the fluctuations in the computed energy values to make the NGC less sensitive to sudden variations in noise energy. The output of the Energy Accumulator **340** is

25   coupled to the output of the Noise Estimator **222**.

A block diagram of another embodiment of a Noise Estimator **224** is shown in FIG. 4. The configuration of the Noise Estimator **224** of FIG. 4 is similar to the Noise Estimator **222** of FIG. 3. The input signal to the Noise Estimator **224** is coupled to a Walsh Code Decover **410** where the first stage in

30   processing a noise estimate is performed. The Walsh Code Decover **410** despreads and decovers the input signal using a predetermined code. The only constraints on the predetermined code are that there are an equal number of ones and zeros. In one embodiment, the code used to despread and decover the input signal is "++--". Here, as in the previous Noise Estimator **222**

35   embodiment, binary signals are represented with "+" or "-" values and "+" may represent a "0" and "-" may represent a "1". Ideally, the despreading code does not duplicate any code used to spread the input signal. In a communication system operating in accordance with the IS-95 standard, the reverse link does not spread each individual signal with a Walsh code. In an IS-95 standard

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reverse link, one of sixty four possible orthogonal Walsh codes is transmitted for each group of six code symbols. Thus, there may not be an orthogonal Walsh code used to despread the input signal that ensures no correlation with the input signal. The output of the Walsh Code Decover **410** is coupled to a

5   noise accumulator **420**. The noise accumulator **420** is configured to accumulate the despread signal over the length of the Walsh code used in the despreading process. The noise accumulator **420** is configured to accumulate four consecutive samples when the despreading code is "++--". The output of the noise accumulator **420** is coupled to an Energy Computation **430** where the

10 energy of the accumulated samples is calculated. Where the input signal is a quadrature signal, as is used in CDMA systems, the energy can be calculated as the sum of the squares of the I and Q signal components. The output of the Energy Computation **430** is coupled to an Energy Accumulator **440** where a predetermined number of energy calculations are accumulated. The output of

15 the Energy Accumulator **440** is coupled to the output of the Noise Estimator **440**.

Fluctuations in the pilot energy are minimized because the NGC operates only on noise. The noise level is estimated by multiplying the received signal by an unassigned Walsh code. When a conventional AGC loop alone is

20 used to adjust the signal level, the pilot energy coupled to the signal processing stages will vary depending on the composite energy of the received signal. One problem identified with adjusting the received signal level with only an AGC loop is seen where a signal is transmitted on an orthogonal CDMA channel at a high power level relative to the pilot and remaining active

25 channels. In this condition, the AGC loop normally reduces the signal power incident on the signal processing stages. In a CDMA system incorporating burst data transmission, the burst nature of the data channel causes a corresponding fluctuation in the received signal level at the signal processing stages because of AGC effects. However, in a CDMA environment, the

30 orthogonal channels have minimal effect on the signal processing of desired code channel because of the orthogonal nature of the signal. Thus, the AGC effectively reduces the desired received signal level to a level below the optimal level. In contrast, the NGC loop only reduces the received signal level when the noise in the received signal increases relative to the desired code channel.

35 A flow chart of a method of correcting a received input signal using noise gain control **500** is shown in FIG. 5. The method starts by receiving communication signals **502**. The communication signals are then processed in an AGC loop **510** before being coupled to a noise estimator **520**. The AGC loop is configured to maintain the received signals about an AGC set point, within

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the limits of the abilities of the AGC loop. The noise estimator calculates an estimate of the noise in the gain controlled signal. Once the noise estimate is determined, the noise estimate is used to calculate a gain correction **530**. In one embodiment, the gain correction is calculated by normalizing the noise estimate

5   to a predetermined noise gain set point and inverting the normalized result. In another embodiment, the gain correction is calculated by subtracting the noise estimate from a predetermined noise gain set point. The method next filters the gain correction **540** to minimize the ability of the gain correction to make sudden changes. The filtered gain correction is next accumulated **550** to

10   achieve an aggregate, or accumulated, gain correction. The accumulated gain correction is then used to scale the output of the AGC signal **560** for subsequent receiver processing **570** of the AGC output signals.

An embodiment of a method of noise estimating **600** is shown in FIG. 6. The noise estimator method **600** first receives an input signal **602**. Here, the

15   input signal may be the scaled output from an earlier AGC stage used within a receiver. The method next despreads the input signal **610** using a Walsh code or other predetermined code having a predetermined length. In a first embodiment, the input signal is despread using a Walsh code having a length of sixteen chips. In another embodiment, the Walsh code used to despread the

20   input signal is "++++--------++++", where binary signals are represented with "+" or "-" values and "+" may represent a "0" and "-" may represent a "1". In an alternative embodiment, "+" may represent a "1" and "-" may represent a "0". In another embodiment, the code used to despread the input signal is a code of even length having an equal number of "+" and "-" chips. In another

25   embodiment, the code used to despread the input signal is "++--".

Once the method despreads the input signal **610** the method next accumulates the despread output over a predetermined number of samples **620**. In one embodiment the predetermined number of samples is equal to the despread code length. In one embodiment, the predetermined number of

30   samples is sixteen, while in another embodiment, the predetermined number of samples is four. The method next computes the energy **630** in the accumulated noise estimate. In one embodiment, the received signal is a quadrature signal and the energy is computed as the sum of the squares of the I and Q noise estimate components. The computed energy value is then accumulated over

35   another predetermined number of energy accumulations **640**. The result of the energy accumulations is the output of the noise estimator method **600**.

The previous description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. The various modifications to these embodiments will be readily apparent to those

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skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of the inventive faculty.

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Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The various illustrative components, blocks, modules, circuits, and steps have been described generally in terms of their functionality. Whether the functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans recognize the interchangeability of hardware and software under these circumstances, and how best to implement the described functionality for each particular application. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

I CLAIM: